Fault-Resistant Partitioning of Secure CPUs for System Co-Verification against Faults*

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[6] Thales DIS, France

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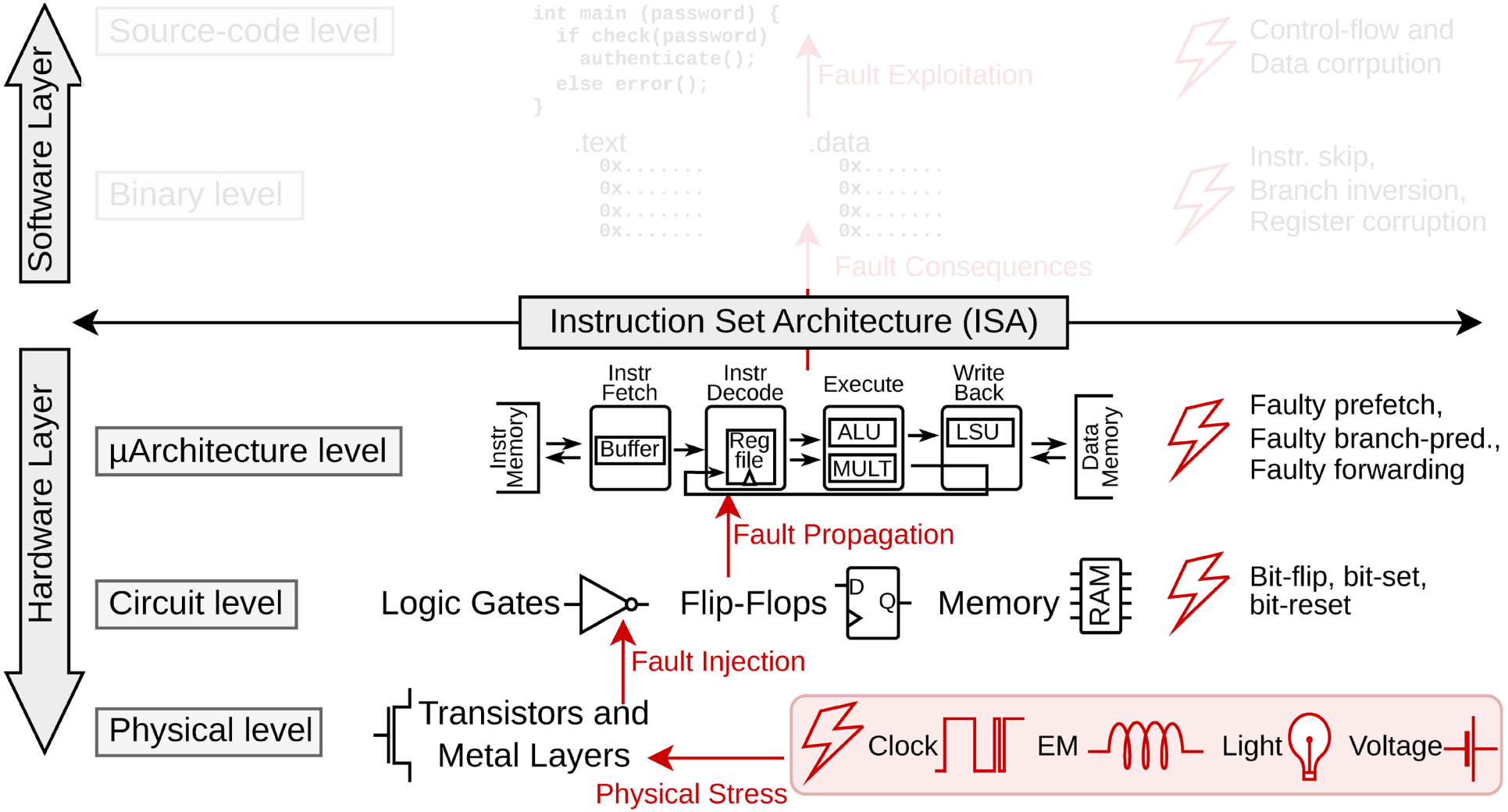
1. Introduction

State of the Art & Motivations

CPU's Abstraction Levels during FIs



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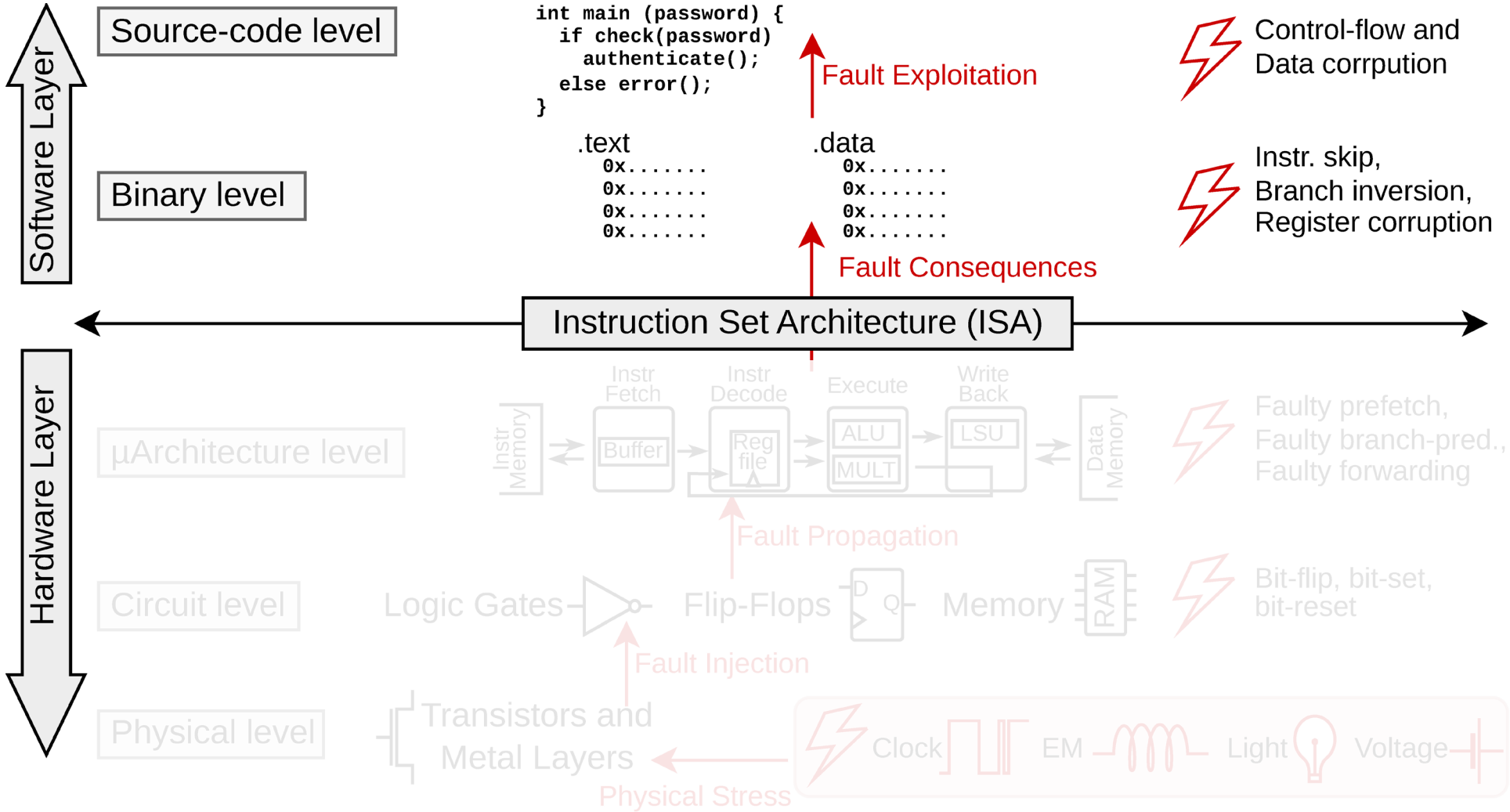
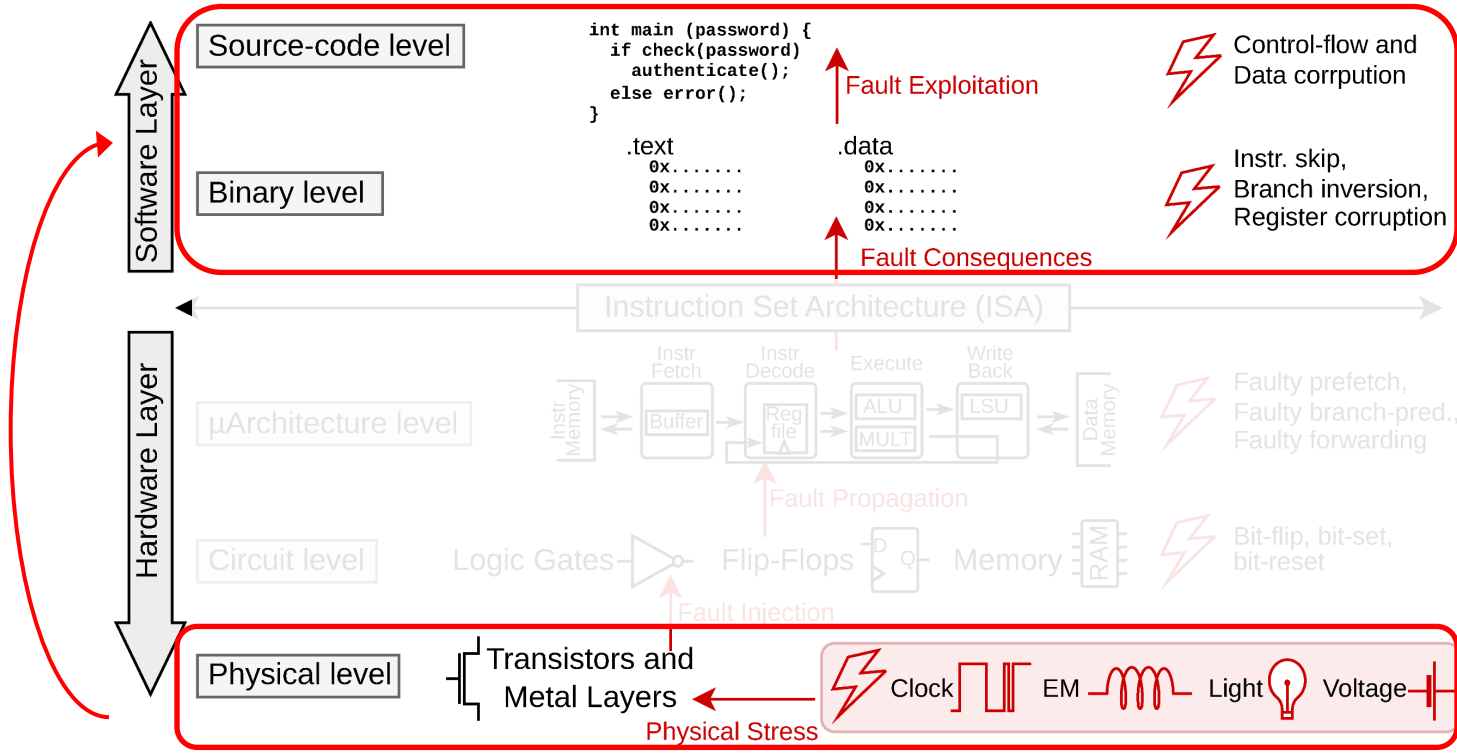


State of the Art & Motivations

Experimental Characterization

- Post-Silicon (often a black box)
- Apply physical stress
- Observe the consequences on software

Observe consequences



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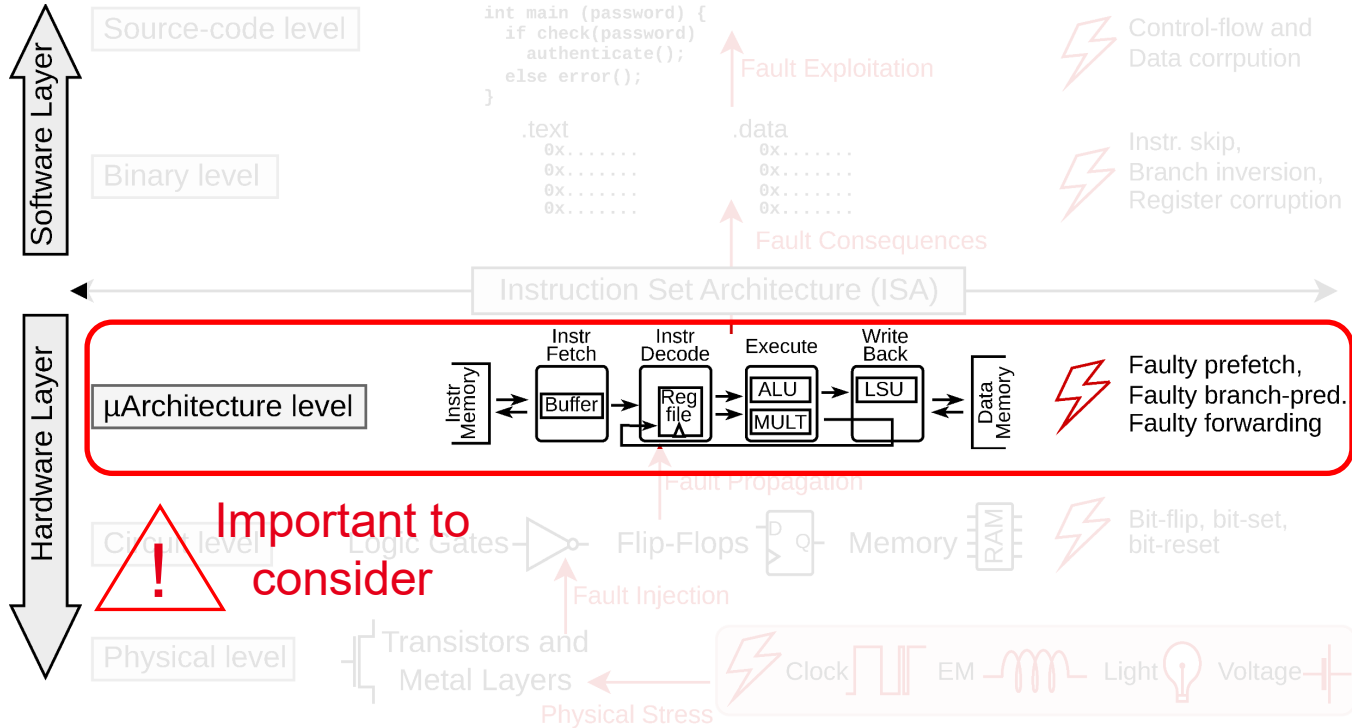
Need to Open the Box

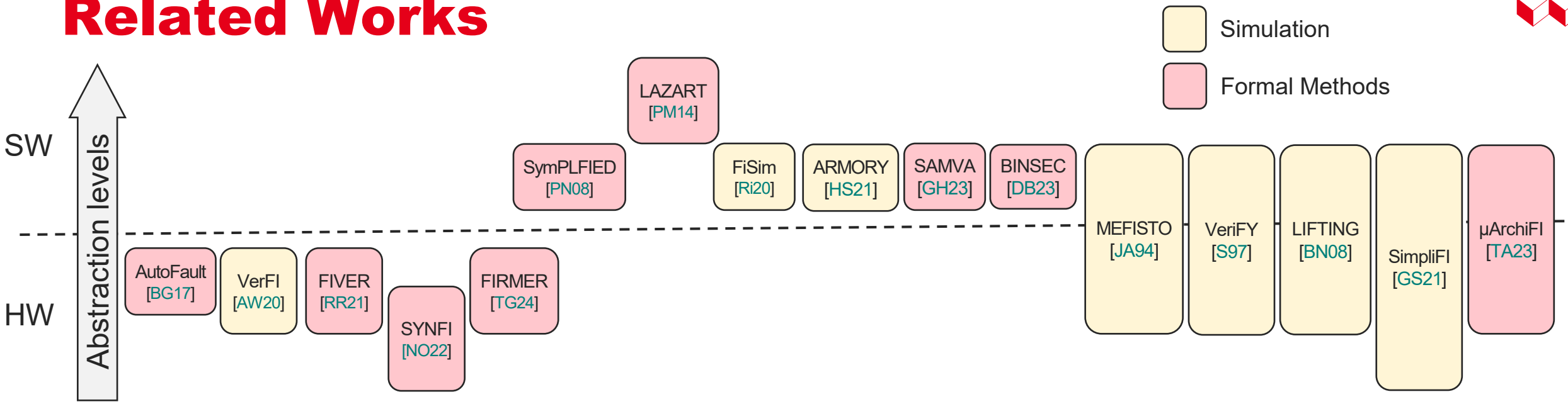
- Unexplainable observed effects [PH19]
- Importance of microarchitectural mechanisms
  - Pipelining [BG11, YG15]
  - Prefetch Buffer [TA22]
  - Forwarding [LB18, LB19]
  - Memory Cache [TB21]



- ***Pre-silicon*** *analyses should now consider* **processor microarchitecture**
- ***Security*** *evaluations require* ***exhaustive*** *methods*

[BG11] Balasch et al. "An in-depth and black-box characterization of the effects of clock glitches on 8-bit MCUs." *FDTC* 2011.
[YG15] Yuce and Schaumont. "Improving fault attacks on embedded software using RISC pipeline characterization." *FDTC* 2015.
[PH19] Proy et al. "A first ISA-level characterization of EM pulse effects on superscalar microarchitectures: a secure software perspective." *ARES* 2019.
[LB18] Laurent et al. "On the importance of analysing microarchitecture for accurate software fault models." *DSD* 2018.
[LB19] Laurent et al. "Fault injection on hidden registers in a risc-v rocket processor and software countermeasures." *DATE* 2019.
[TB21] Trouchkine et al. "Electromagnetic fault injection against a complex CPU, toward new micro-architectural fault models." *Journal of Cryptographic Engineering* 2021.

Related Works



Pre-Silicon Evaluation: Simulation vs Formal Methods

- Simulation: Execute concrete instances of the system
- Formal Methods: Reason on a system model to prove properties

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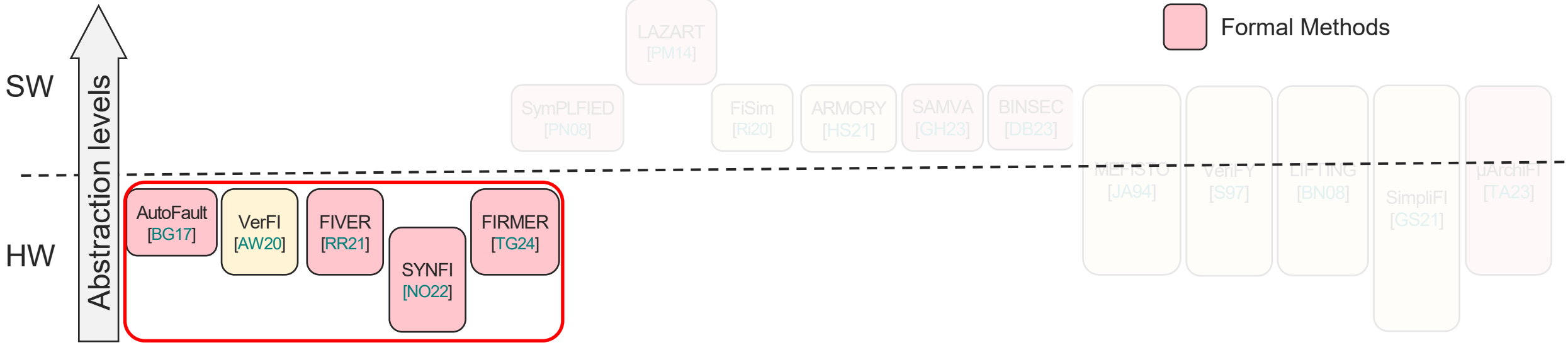

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Hardware Methods

- Dedicated to evaluate crypto circuits
- Compare fault-free vs. faulted circuits
- Performance (FIVER on AES):
  - 1 fault in **22 sec.**
  - 2 faults in **130 hours**

➢ Cannot model program execution

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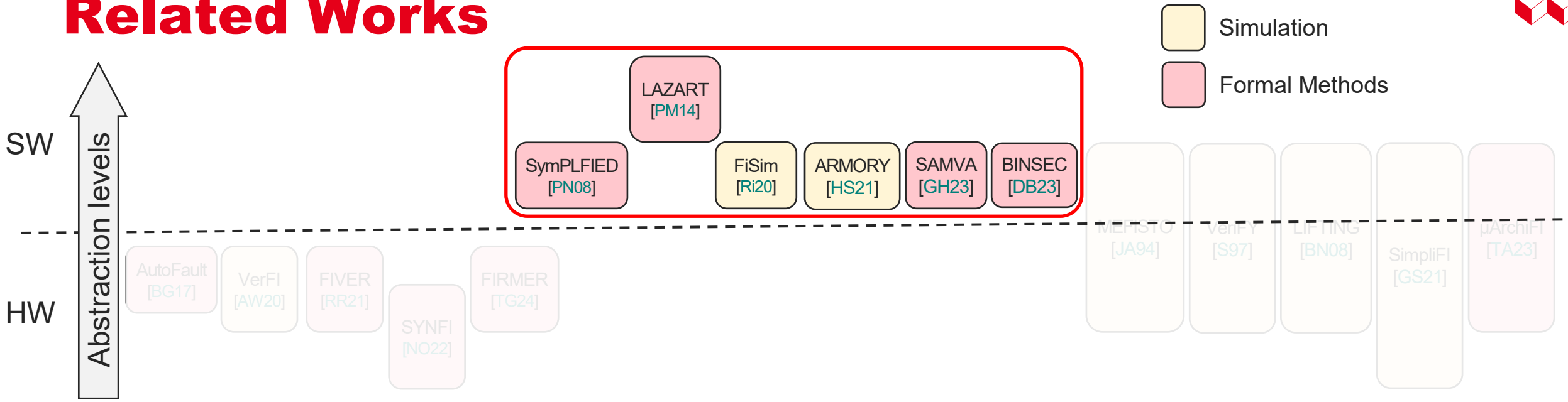

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Software Methods

- ISA fault models, e.g., inst. skip
- Performance (BINSEC):
  - Bootloader: 1 fault in **9 sec.**
  - PIN comp.: 10 faults < **1 sec.**

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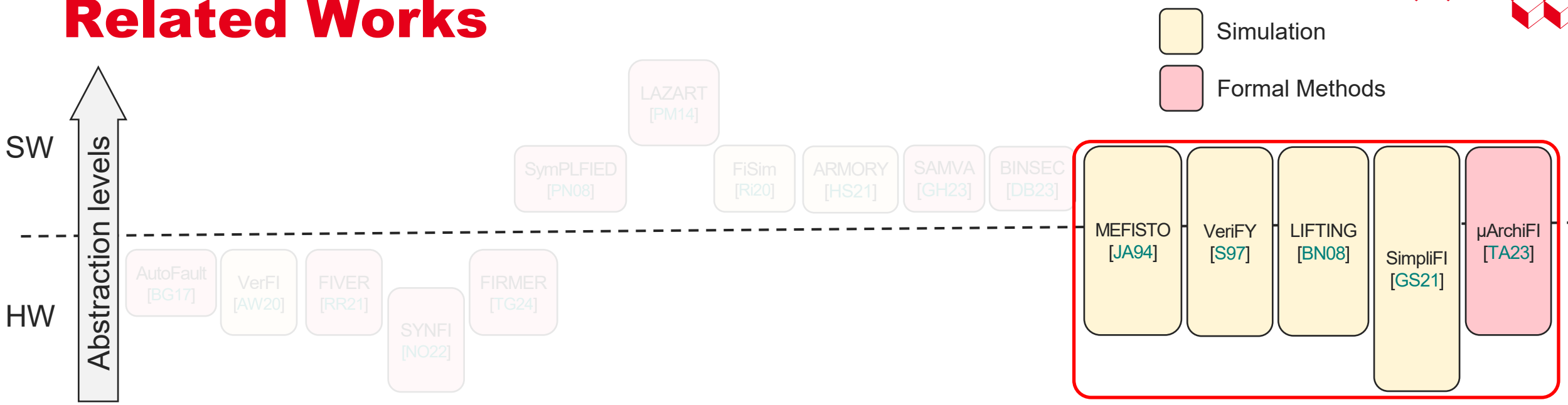

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Combined Methods

- Originally for safety analysis with simulation
- Identify complex interplay between HW and SW
- ➢ Scalability issues (µArchiFI in **14 hours**)
  - 100 instructions
  - Small in-order CPU (46 kGE)
  - 1 fault injection

Problem Statement and Contributions

Observation

- HW- or SW-only evaluations are insufficient

Need

- **Pre-silicon combined HW/SW** analyses
- **Exhaustive** techniques, e.g., formal methods ➔ Security guarantees

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Challenge: State space explosion problem

- *Exploring* **the entire state space ➔ Scalability issues**
- *Addressing scalability is essential for* **practical applicability**

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- *Addressing scalability is essential for* **practical applicability**

Contributions

- **Decompose** HW/SW co-verification ➔ **Contain the state space explosion**
- **Address previously intractable** use cases with our new methodology

Outline

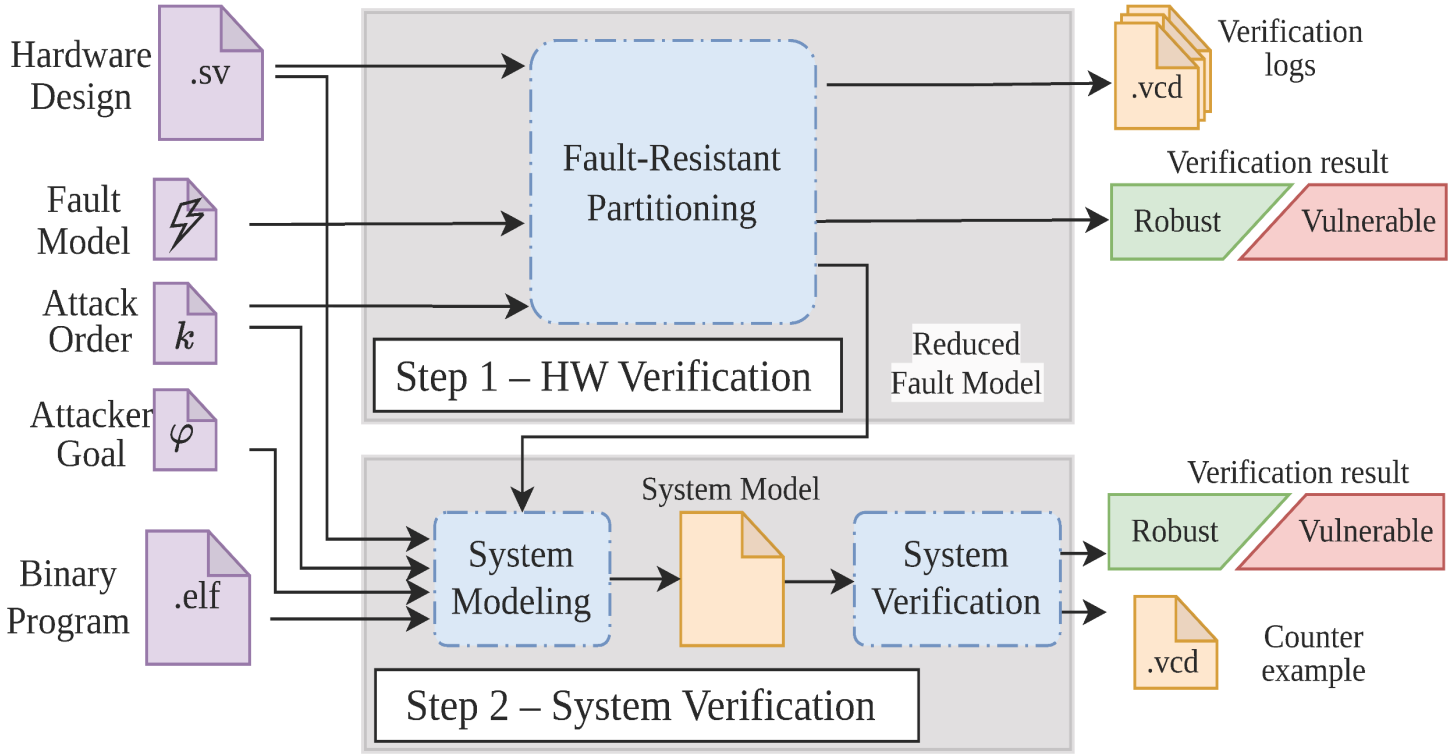
1. Introduction
2. Methodology
3. Validation on Impeccable Circuits
4. Evaluation of OpenTitan
5. Conclusion

2. Methodology

Methodology Overview

Principle

- Security-critical systems implement **HW protections**
- **Preliminary evaluation** of the hardware security
  - Must be run only once
- Faults not detected by HW must be detected by SW



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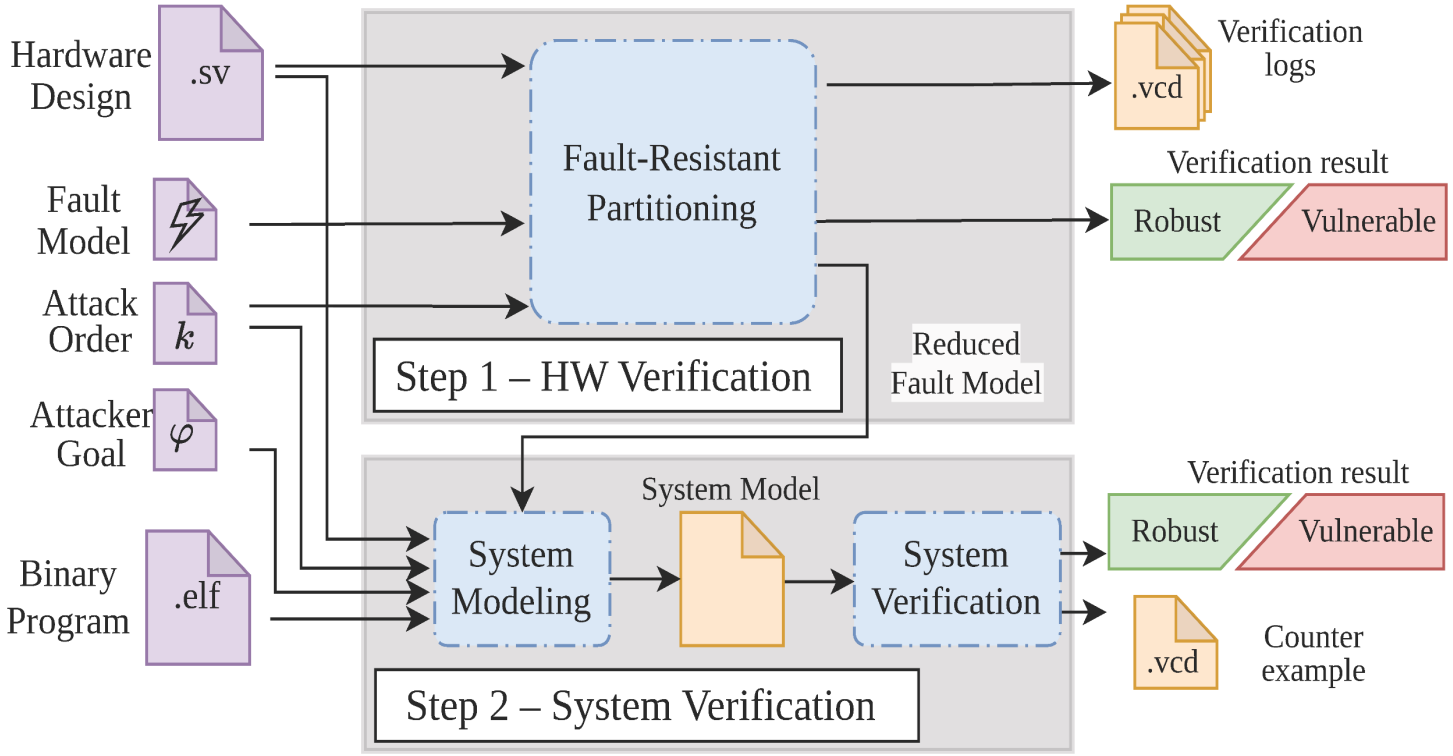
Requirements

➢ Need formal HW security guarantees to remove ineffective faults during SW co-verification

- Existing HW Techniques
  - Compare *fault-free trace* (*golden*) vs. *faulty trac*
  - Only provide **bounded** guarantees → **Insufficient**

- Faults can have long-term effects: e.g., hidden in microarchitectural registers

➢ Need **unbounded guarantees**

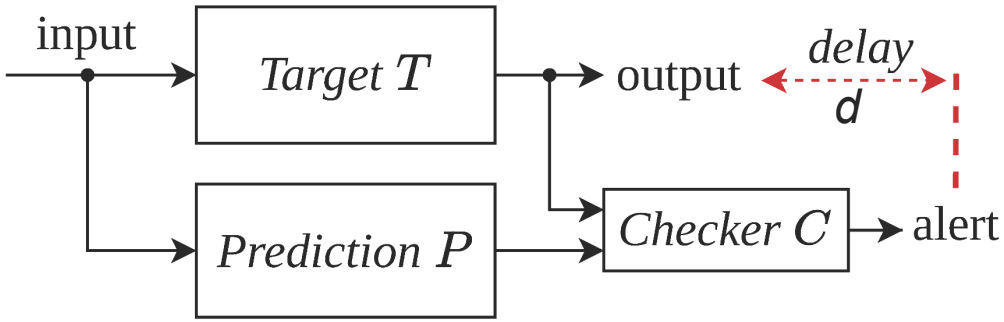


Step 1 — HW Verification

Concurrent Error Detection Scheme

- Spatial redundancy, e.g.,
  - Duplication
  - Triplication
- Informational redundancy e.g.,
  - Error detection codes

➢ Raise an alert on a mismatch (with a potential delay *d*)



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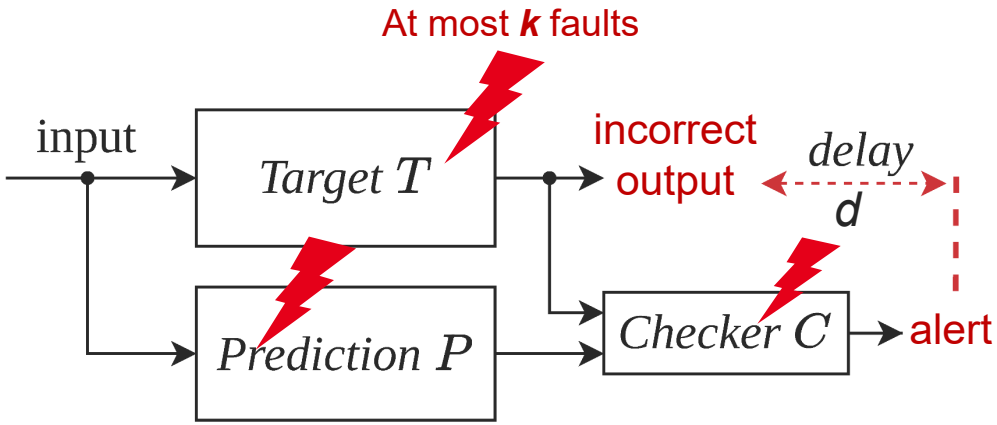


Definition (*k*-Fault Security)

Assumptions

- At most ***k*** faults are injected in the circuit

Guarantees

- Circuit's outputs are correct, or an alert is raised after at most ***d*** clock cycles

Fault-Resistant Partitioning

Contribution

- Build and prove a *fault-resistant partitioning* of registers

Definition (*k*-Fault-Resistant Partitioning)

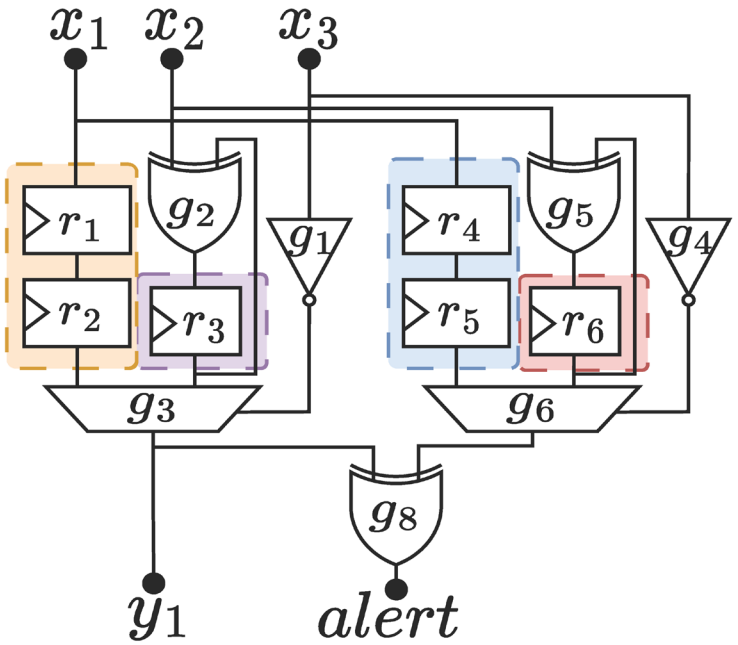
Assumptions

- Maximum budget of k faults, i.e., $k_1 + k_2 \leq k$
- At most k_1 faults in partitions at clock cycle j
- At most k_2 faults in logic gates at clock cycles $[j, j + d]$
- No alert between cycles j and $j + d$

Guarantees

- At most $k_1 + k_2$ faulty partitions at clock cycle $j + 1$
- No corrupted outputs at clock cycle j

Example with *k = 1*



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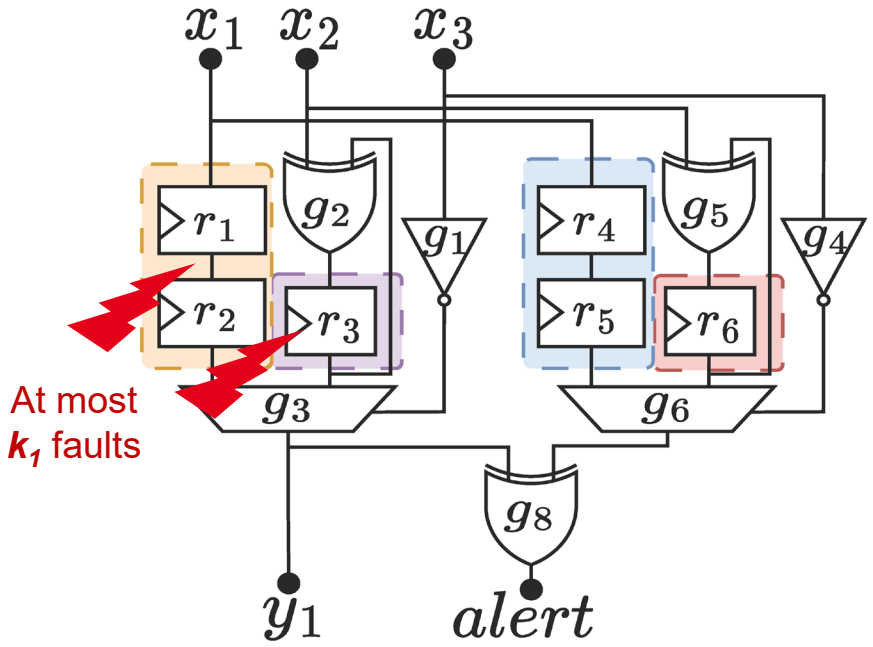

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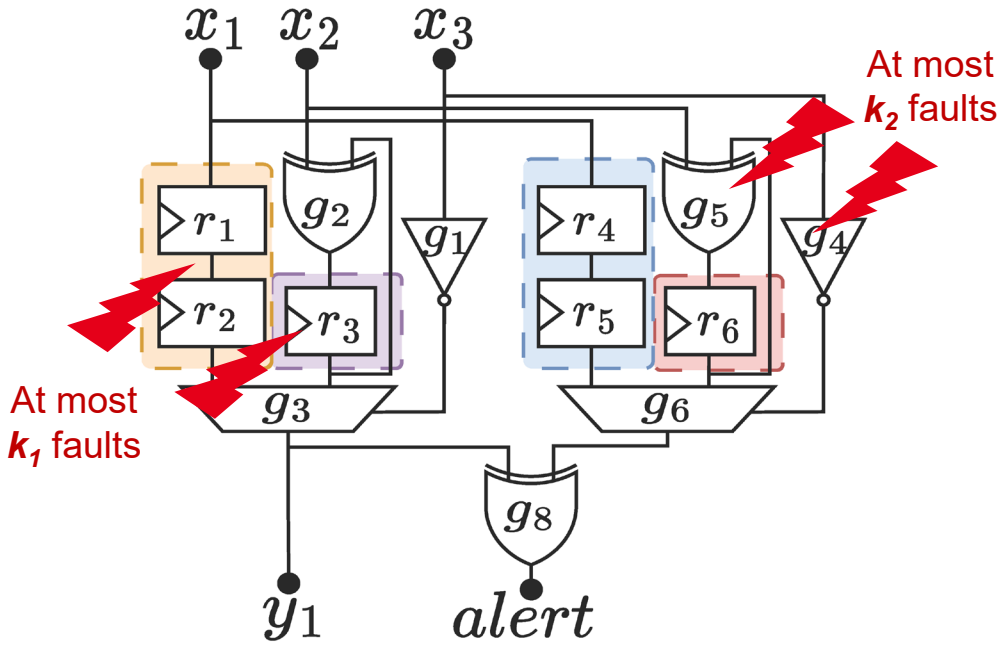

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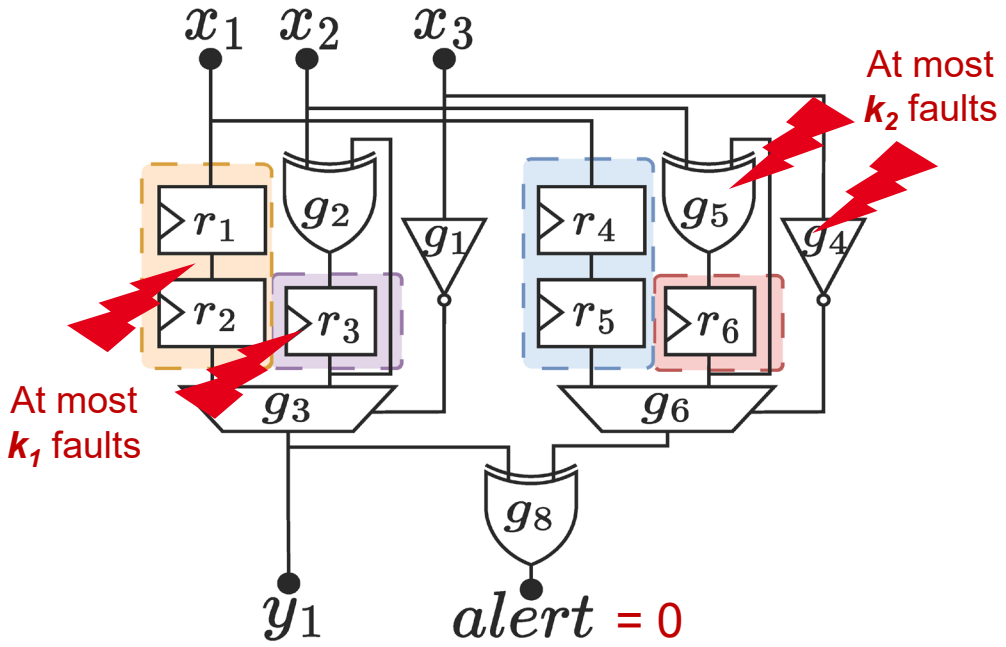

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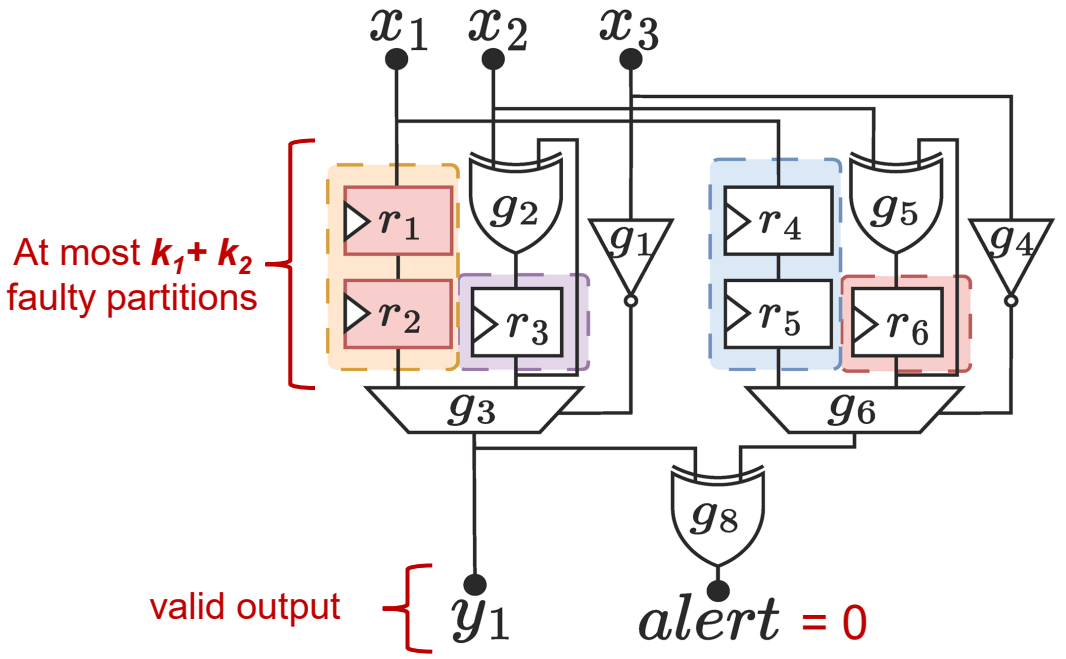

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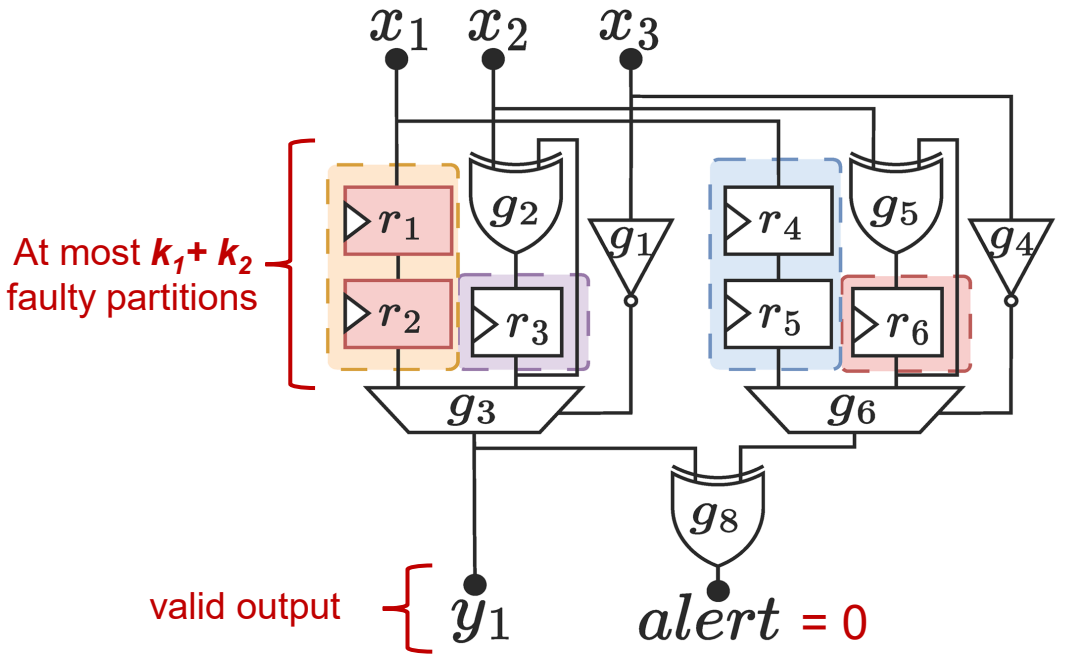

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Theorem

k-fault resistant partitioning ⇒ k-fault security

➢ *Formal definitions and proofs are in the paper*

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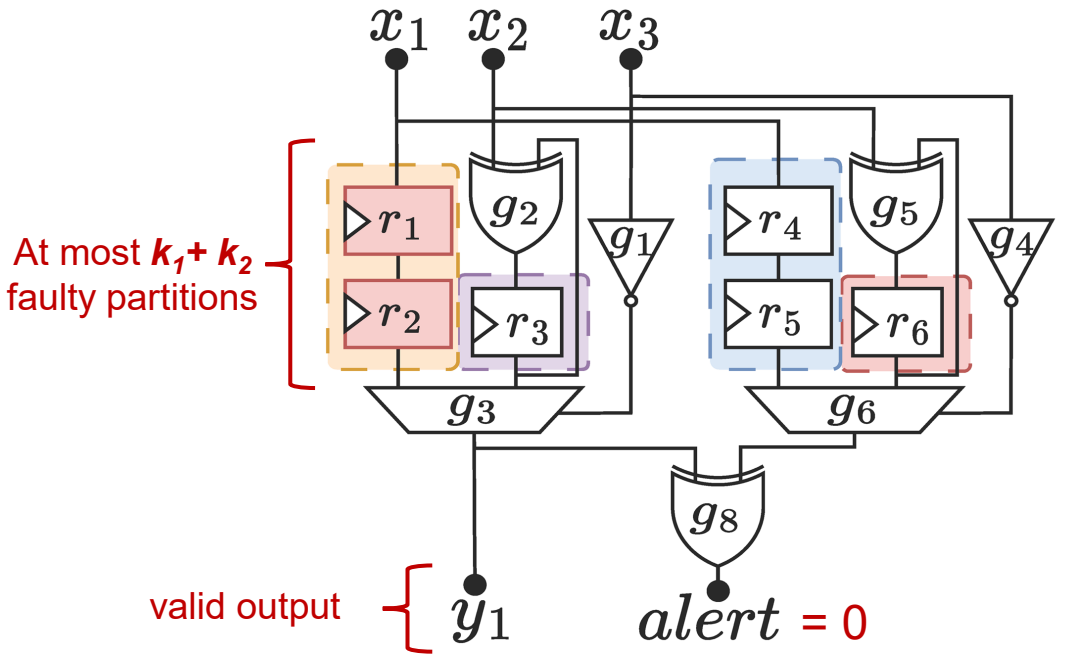

Advantages

- No need to unroll the circuit — fault propagation is abstracted
- Provide unbounded guarantees

Limitations

- Over-approximation of *k*-fault security
- Some circuits are *k*-fault secure, but we cannot prove it

3. Validation on Impeccable Circuits

Validation on Impeccable Circuits

Why Impeccable Circuits?

- No similar work exists on CPUs for comparison
- Validate the first step of our methodology
  - Against prior work like FIVER [RR21]
  - Evaluate verification performance
  - With multiple-fault attacks

Impeccable Circuits [AM19]

- Symmetric Bloc Ciphers (AES, LED, Simon, Skinny …) protected with Error Detection Codes (EDC).
- Designed to detect up to 3 faults (up to 7 faults for AES).
- An error signal is raised on fault detection and circuit outputs are zeroed out.

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Experimental Results

- With 2 faults, we **prove** security of:
  - Skinny in **10 sec.**
  - AES in **4 hours** — FIVER took **130 hours**
- With 3 faults (assuming no faults in the checker), we **prove** security of:
  - Skinny in **40 sec.**
  - AES in **55 hours** — **never** been done before

[AM19] Aghaie, Anita, et al. "Impeccable circuits." *IEEE Transactions on Computers* 2019.
[RR21] Richter-Brockmann, Jan, et al. "Fiver–robust verification of countermeasures against fault injections". *CHES 2021.*

4. OpenTitan Evaluation

OpenTitan's Processor: Secure Ibex

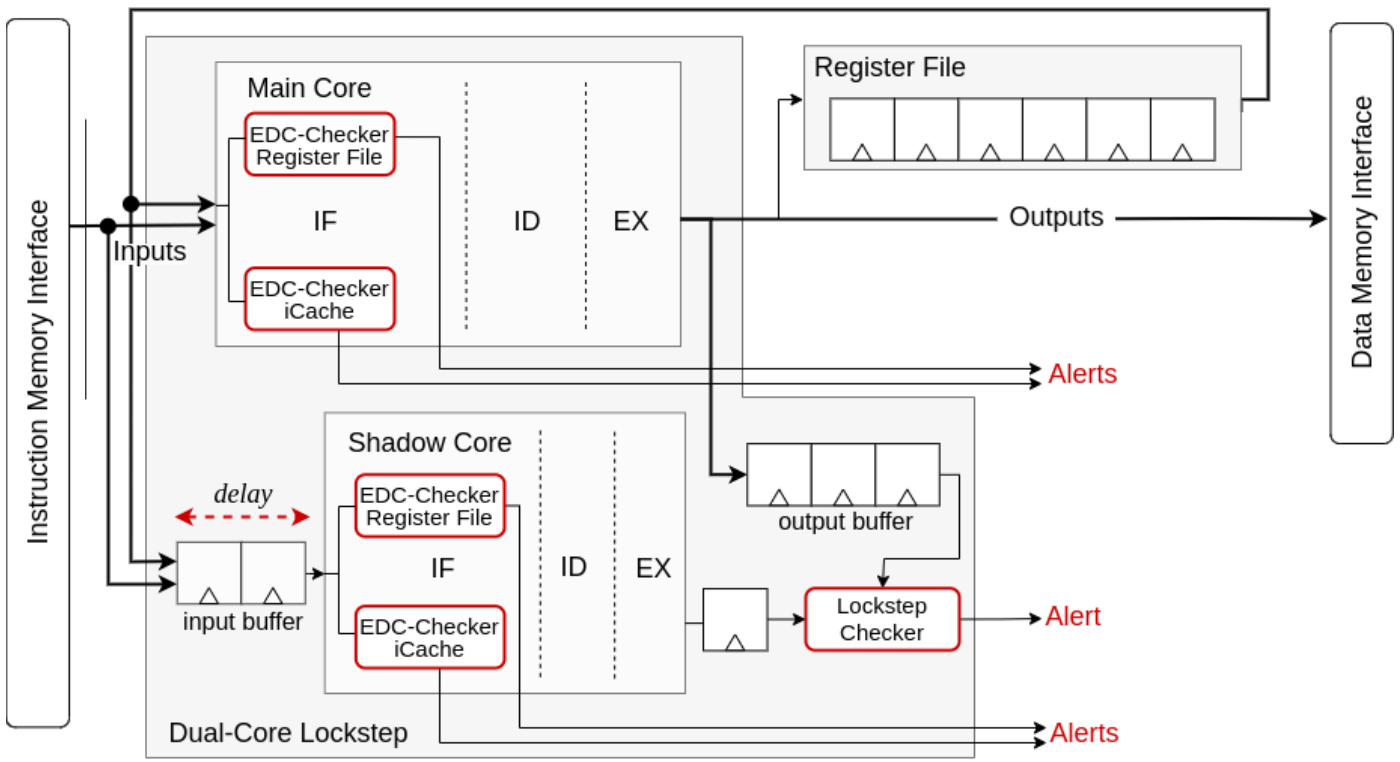


Figure - Secure Ibex Block Diagram

Secure Element OpenTitan [JR18]

opentitan

Secure-Ibex (development version) [Lo18]

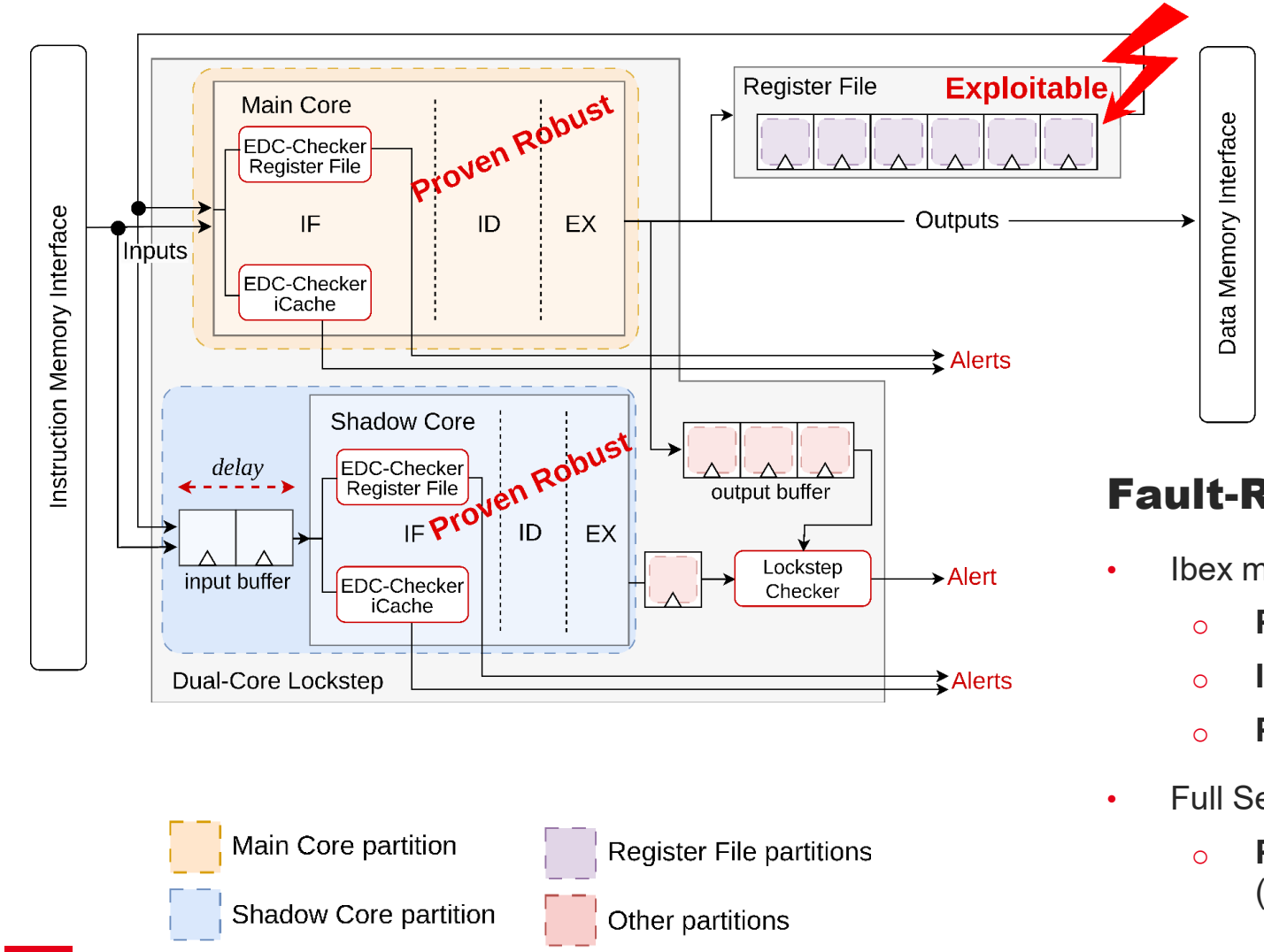
- RISC-V processor, 3 stages, in-order
- Concurrent Error Detection schemes, e.g.,
  - Dual Core Lockstep (DCLS) with delay d
  - Error Detection Codes in Register File

Fault Model

- Attacker with physical access to the processor
- Single transient bit-flip everywhere at any time

[JR18] Johnson, Scott, et al. "Titan: enabling a transparent silicon root of trust for cloud." *Hot Chips: A Symposium on High Performance Chips*. Vol. 194. 2018.
[Lo18] lowRISC. Ibex RISC-V Core github repository. https://github.com/lowRISC/ibex. Accessed: February 22, 2024.

HW Evaluation: Results



Fault-Resistant Partitioning Results

- Ibex modules
  - **Prove** 1-fault security of DCLS in **26 hours**
  - **Identify** 172 exploitable locations in Reg. File in **1 min 30**
  - **Prove** 3-seq.-fault security of Reg. File in **12 mins**
- Full Secure Ibex
  - **Prove** 1-fault security in **42 hours (+ 26 h)**
    (assuming no faults in the 172 exploitable locations identified)

System Co-Verif: SW Case Studies + Results

First Stage of Secure Boot

- *Provided by the OpenTitan project*

- Check authenticity and integrity of the next boot stage
- Implement software protections e.g.,
  - Step counters
  - Test duplications

- Goal: **Bypass memory signature check**
- # instructions: **2 526**
- # faults: **122 048**
- Performance: **2.5 hours** (8 threads)
- Results: **Secure**

[DP16] Dureuil, Louis, et al. "FISSC: A fault injection and simulation secure collection." *SAFECOMP* 2016.
[Ko19] kokke. Tiny AES, release 1.0. https://github.com/kokke/tiny-AES-c, 2019. Accessed: February 22, 2024.

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VerifyPIN [DP16]

- ***Not*** *provided by the OpenTitan project*

- Compare two PINs for authentication
- 8 versions with various mix of protections

- Goal1: **Bypass authentication**
- Goal2: **Increase max number of tries**
- # instructions: **187**
- # faults: **7 424**
- Performance: **6 mins** (1 thread)
- Results: **Insecure**

DFA on tiny AES [Ko19]

- ***Not*** *provided by the OpenTitan project*

- SW implementation of AES

- Goal1: **DFA on key schedule**
- # instructions: **221**
- # faults: **5 760**
- Performance: **7 mins** (2 threads)
- Results: **Insecure**

- Goal2: **DFA on 7th AES round**
- # instructions: **1 144**
- # faults: **38 912**
- Performance: **29 mins** (8 threads)
- Results: **Insecure**

[DP16] Dureuil, Louis, et al. "FISSC: A fault injection and simulation secure collection." *SAFECOMP* 2016.
[Ko19] kokke. Tiny AES, release 1.0. https://github.com/kokke/tiny-AES-c, 2019. Accessed: February 22, 2024.

4. Conclusion

Conclusion

Co-verification Methodology

- **Two-step** methodology to evaluate fault security
  - Step 1 — **Preliminary analysis** of HW countermeasures
  - Step 2 — **Remaining faults** not detected by the HW are evaluated with the SW

Step 1 — Fault-Resistant Partitioning

- Provide **unbounded security guarantees** which are crucial for SW co-verification
- **Outperform** state-of-the-art solvers like FIVER
- First work to evaluate AES against **3 faults**

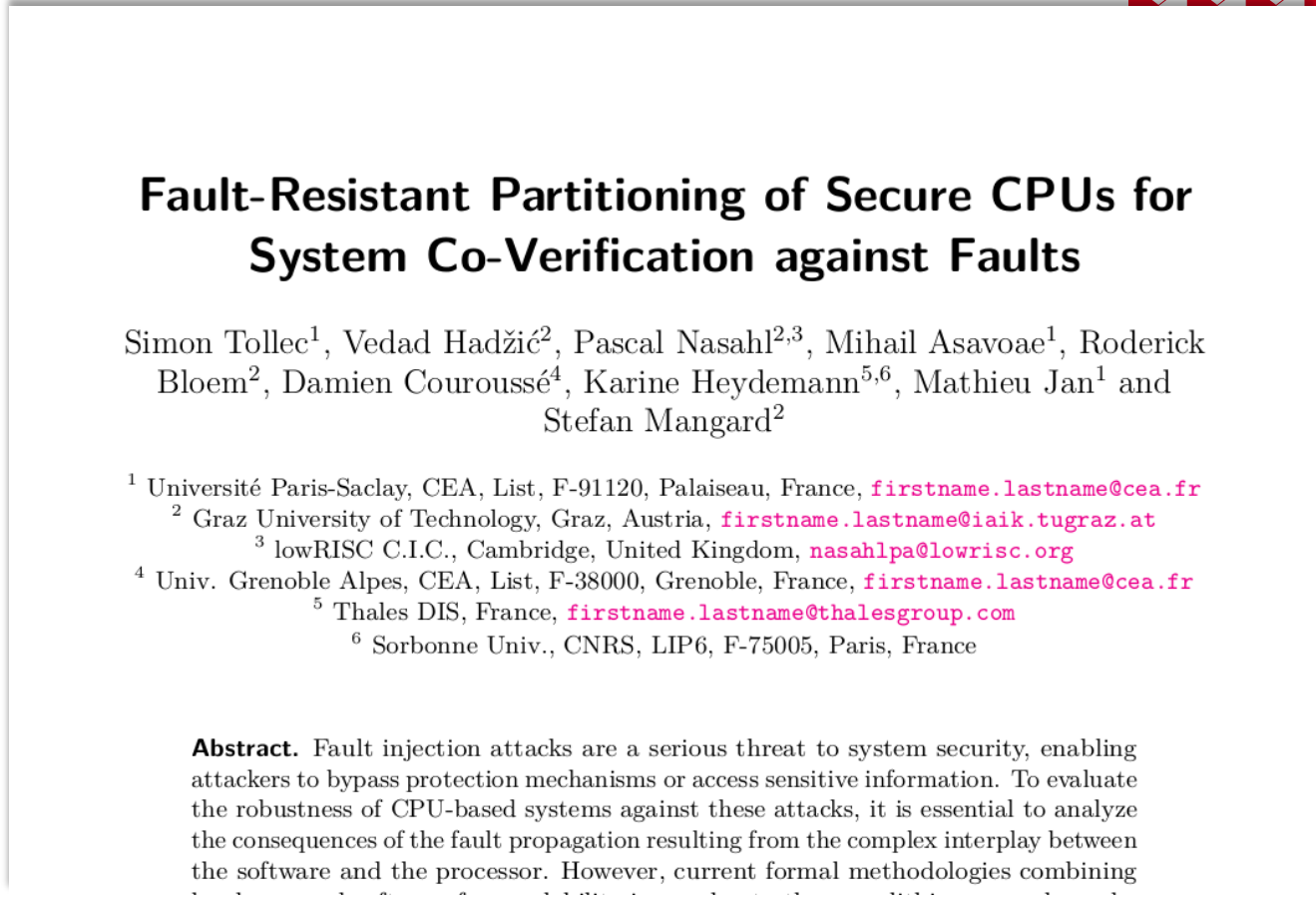
Step 2 — System co-verification

- Address **previously intractable** software verification of thousands of instructions
- First work to prove the security of the first stage of a **secure boot against fault attacks**

Thank you

Questions?

Come and see my poster



Fault-Resistant Partitioning of Secure CPUs for System Co-Verification against Faults

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Abstract. Fault injection attacks are a serious threat to system security, enabling attackers to bypass protection mechanisms or access sensitive information. To evaluate the robustness of CPU-based systems against these attacks, it is essential to analyze the consequences of the fault propagation resulting from the complex interplay between the software and the processor. However, current formal methodologies combining

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Implementation 1/2

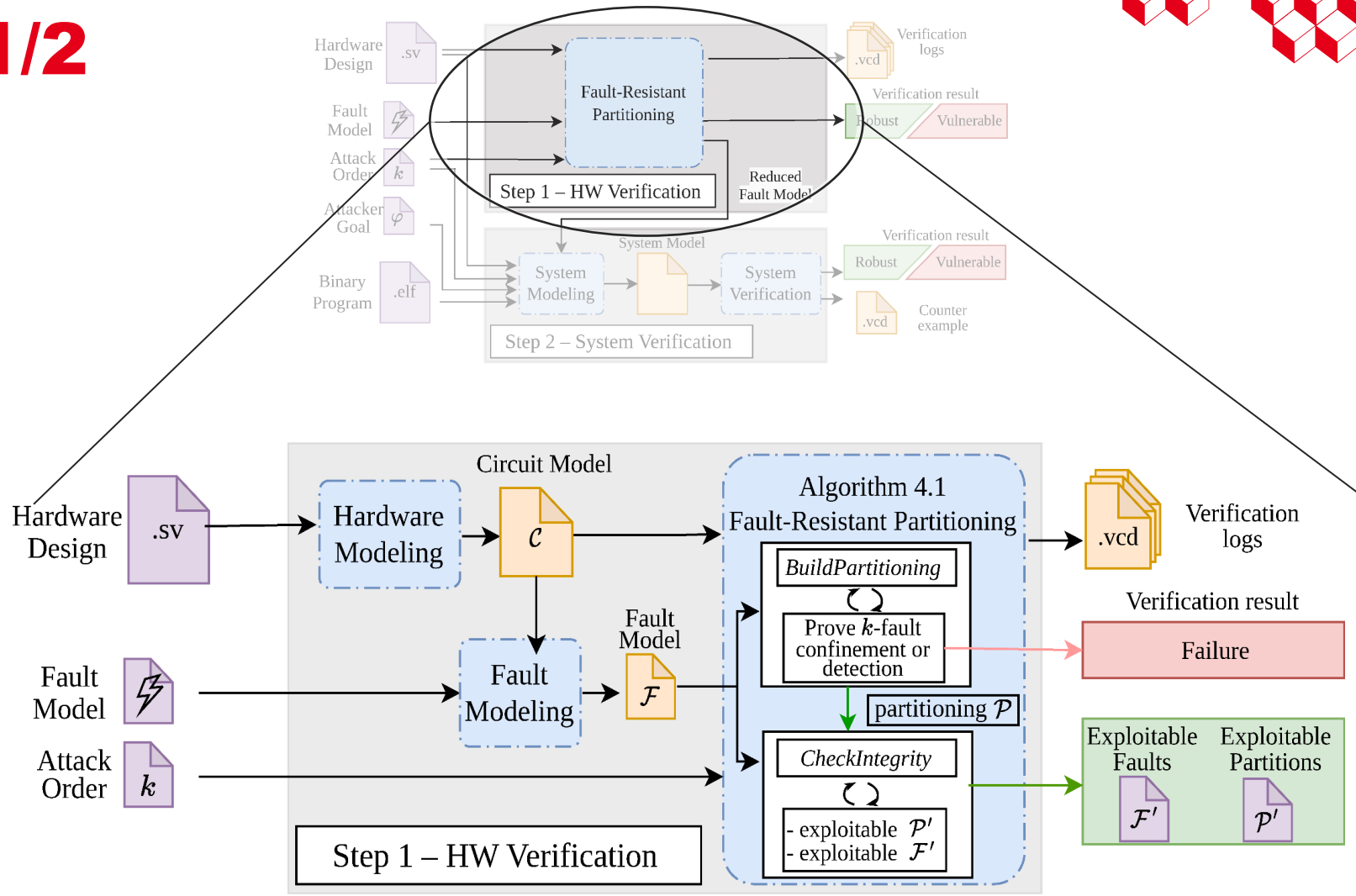
Fault-Resistant Partitioning

1. *BuildPartitioning* procedure
2. *CheckIntegrity* procedure

➢ Algorithm outputs are **unprotected/ exploitable** faults

- Rely on CaDiCaL SAT solver [Bi20]
- About 4 000 lines of code
- Open-source:

https://github.com/CEA-LIST/Fault-Resistant-Partitioning



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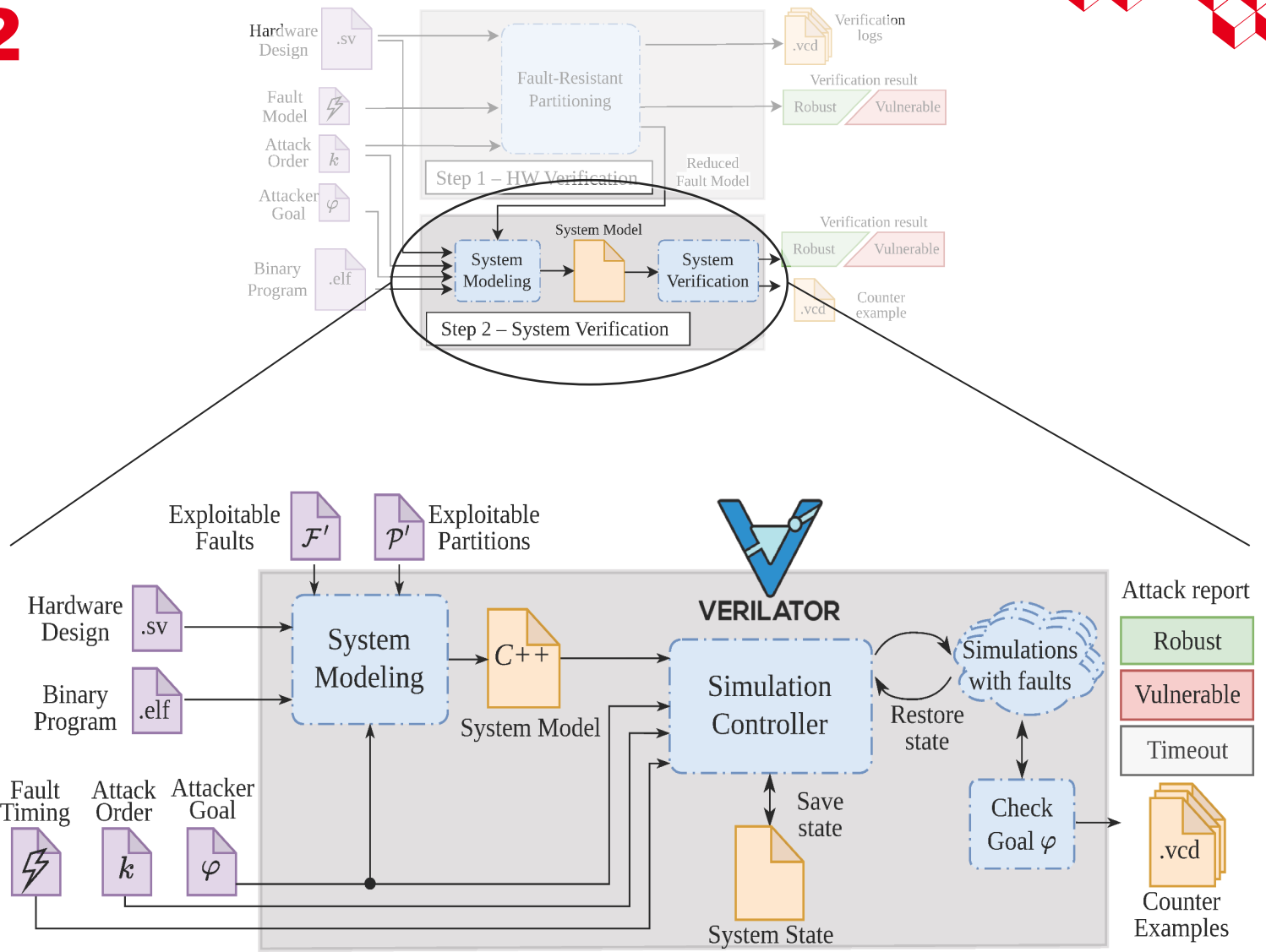
Implementation 2/2

System Co-Verification

- Evaluate whether exploitable faults with SW
- Based on the Verilator environment
- Exhaustively simulates exploitable faults



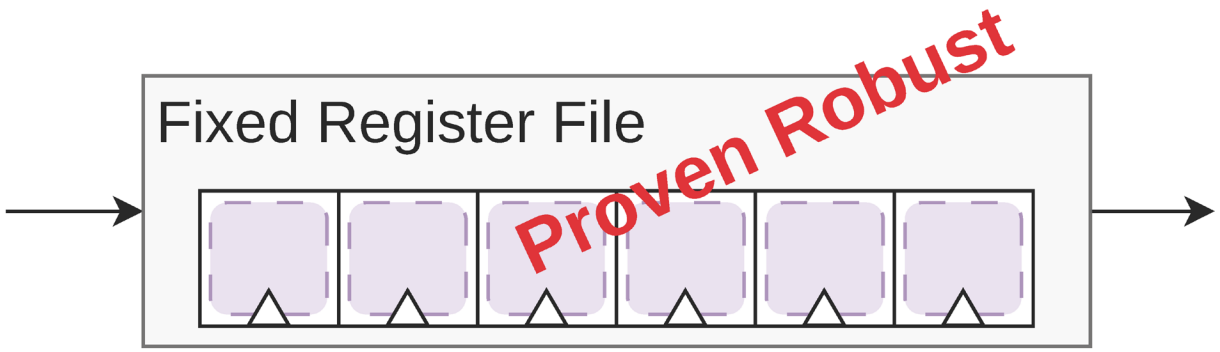
Fix of the Register File

Vulnerability Report

- 172 exploitable faults — allow reading from an incorrect register location
- We **reported the vulnerability** to the OpenTitan project
- They acknowledged our findings

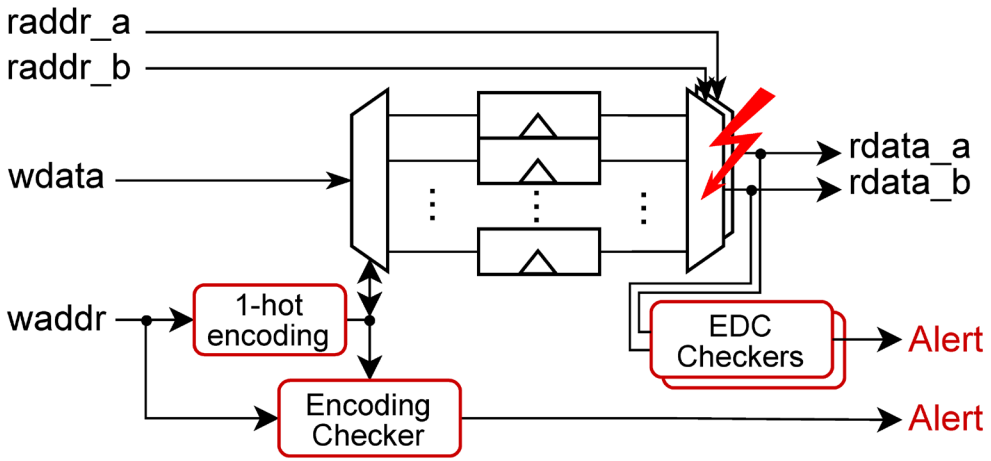
Vulnerability Fix

- We **proposed a security fix** and formally **prove it** using our methodology
- Our fix was integrated into the OpenTitan project
- **Secure Ibex** is now **proven 1-fault secure** unconditionally of the executed software

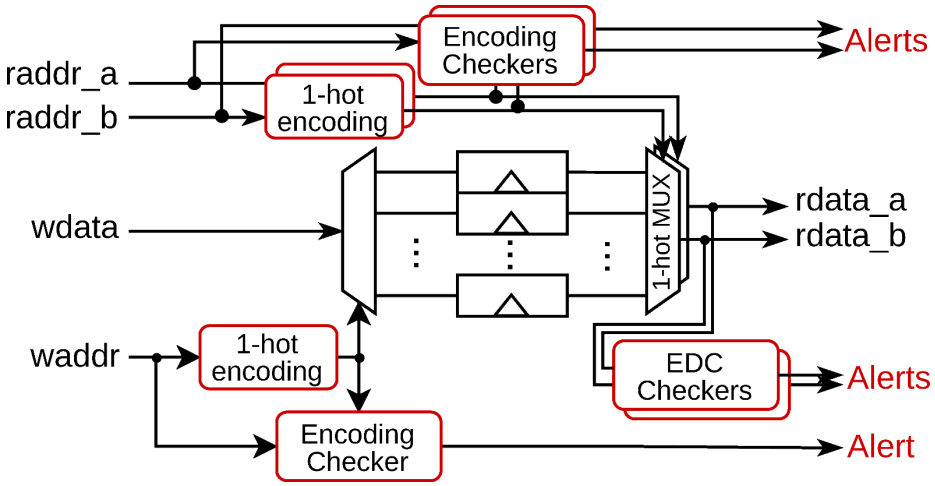


Hardware Fix + Prove

Register File Vulnerability



Register File Security Fix



Fault Propagation and Hidden Faults